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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,936	09/09/2003	Richard M. Fastow	AMD-H0561	3102

7590 03/23/2005

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,936	FASTOW, RICHARD M.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *15-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the communications dated 09/09/2003, claims 1-20 are active in this application.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

Group I: Claims 1-14, drawn to semiconductor devices, classified in class 257, subclass 315.

Group II: Claims 15-20, drawn to processes of making semiconductor devices, classified in class 438, and subclass 257.

3. The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of following can be shown: (1) that the process as claimed can be use to make other and materially different product or by hand, or (2) that the product as claimed can be made by another and materially different process. (MPEP § 806.05(f)). In the instant case, unpatentability of the group I invention would not necessarily imply unpatentability of the group II invention, since the device of the group I invention could be made by other and materially different processes from those of the group II invention.

4. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, the fields of search are not co-extensive. Therefore, separate examination would be required and restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Attorney William A. Zarbis on 03/16/2005, a provisional election was made without traverse to prosecute the invention of Group I, claims 1-14. Affirmation of this election of claims must be made by applicant in replying to this Office action.

Claims 15-20 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

6. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a diligently filed petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(h).

Specification

7. The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claim(s) 1, 7, 10, and 13 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,750,502 to Sandhu et al.

Regarding claim 1, Sandhu discloses a flash memory cell, as shown in figs.10-11, comprising:

a substrate 10 comprising a source 72 and a drain 74;

a gate element ((26/34/36), and

a dielectric layer 24 between said substrate 10 and said gate element, said dielectric layer 24 comprising a dielectric material having a dielectric constant greater than that of silicon dioxide. See col. 4, lines 36-52.

Regarding claim 7, Sandhu discloses the flash memory cell wherein said dielectric material comprises a metal oxide. See col. 4, lines 36-53.

Regarding claim 10, Sandhu discloses a flash memory array, as shown in figs. 10-12, comprising memory cells, wherein a memory cell comprises:

a substrate 10 comprising a source 72 and a drain 74;

a gate element (26/34/36); and

a tunnel oxide layer 24 between said substrate 10 and said gate element, said tunnel oxide layer 24 comprising a dielectric material having a dielectric constant greater than that of silicon dioxide. See col. 4, lines 36-53.

Regarding claim 13, Sandhu discloses the flash memory array of Claim 10 wherein said dielectric material comprises a metal oxide. See col. 4, lines 36-53.

10. Claim(s) 1-8 and 10-14 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,803,275 to Park et al.

Regarding claim 1, Park discloses a flash memory cell, as shown in fig. 1, comprising:

a substrate 16 comprising a source 12 and a drain 14;

a gate element 22, and

a dielectric layer 30 (or 24) between said substrate 16 and said gate element 22, said dielectric layer 24 comprising a dielectric material having a dielectric constant greater than that of silicon dioxide. See col. 4, lines 1-52; col. 6, line 5 to col. 7, line 23; col. 17, line 24 to col. 18, line 19; and col. 19, lines 6-67.

Regarding claim 2, Park discloses the flash memory cell further comprising a layer 28 comprising interfacing material between said dielectric layer 30 and said substrate 16. See fig. 1 and col. 6, line 5 to col. 7, line 23.

Regarding claim 3, Park discloses the flash memory cell wherein said interfacing material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 6, line 5 to col. 7, line 23.

Regarding claim 4, Park discloses the flash memory cell further comprising a layer 32 comprising interfacing material between said dielectric layer 30 and said gate element 22. See fig. 1 and col. 19, lines 6-67.

Regarding claim 5, Park discloses the flash memory cell wherein said interfacing material is selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 19, lines 9-15 and col. 6, line 5 to col. 7, line 23.

Regarding claim 6, Park discloses the flash memory cell wherein said dielectric layer 30 further comprises a first layer 28 comprising a first interfacing material and a second layer 32 comprising a second interfacing material, wherein said dielectric material is layered between said first and second layers. See fig. 1 and col. 6, line 5 to col. 7, line 23; col. 17, line 24 to col. 18, line 19; and col. 19, lines 6-67.

Regarding claim 7, Park discloses the flash memory cell wherein said dielectric material comprises a metal oxide. See col. 17, line 24 to col. 18, line 19.

Regarding claim 8, Park discloses the flash memory cell wherein said dielectric layer 30 comprises a composite of a metal oxide and a material selected from the group consisting of silicon dioxide, silicon oxynitride, and silicon oxynitrate. See col. 17, lines 24-60.

Regarding claim 10, Park discloses a flash memory array, as shown in fig. 1, comprising memory cells, wherein a memory cell comprises:

a substrate 16 comprising a source 12 and a drain 14;

a gate element 22; and

a tunnel oxide layer 24 between said substrate 16 and said gate element 30, said tunnel oxide layer 24 comprising a dielectric material 30 having a dielectric constant greater than that of silicon dioxide. See col. 2, lines 33-43; col. 4, lines 1-52; col. 6, line 5 to col. 7, line 23; col. 17, line 24 to col. 18, line 19; and col. 19, lines 6-67.

Regarding claim 11, Park discloses the flash memory array wherein said tunnel oxide layer 24 further comprises a first layer 28 comprising a first interfacing material and a second layer 32 comprising a second interfacing material, wherein said dielectric material 30 is layered between said fist and second layers 28/32. See fig. 1, and col. 6, line 5 to col. 7, line 23; col. 17, line 24 to col. 18, line 19; and col. 19, lines 6-67.

Regarding claim 12, Park discloses the flash memory array wherein said first interfacing material and said second interfacing material are selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 6, line 5 to col. 7, line 23; and col. 19, lines 6-67.

Regarding claim 13, Park discloses the flash memory array wherein said dielectric material comprises a metal oxide. See col. 17, line 24 to col. 18, line 19.

Regarding claim 14, Park discloses the flash memory array wherein said tunnel oxide layer comprises a composite of a metal oxide and a material selected from the group consisting of silicon dioxide, silicon oxynitride and silicon oxynitrate. See col. 6, line 5 to col. 7, line 23; col. 17, line 24 to col. 18, line 19; and col. 19, lines 6-67.

11. Claim(s) 1 and 9 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,713,810 to Bhattacharyya.

Regarding claim 1, Bhattacharyya discloses a flash memory cell, as shown in figs. 10-11, comprising:

a substrate 12 comprising a source and a drain;

a gate element (204/206/208), and

a dielectric layer 52 between said substrate 12 and said gate element, said dielectric layer 52 comprising a dielectric material (silicon nitride, col. 12, lines 55-58) having a dielectric constant (k ~ 6 - 7) greater than that of silicon dioxide (k = 3.9). See col. 12, lines 29-65 (for further properties of silicon dioxide and silicon nitride and their dielectric constants, see the "Semiconductor Glossary" at http://www.semiconductorglossary.com/).

Regarding claim 9, Bhattacharyya discloses the flash memory cell wherein said substrate 12 comprises silicon and wherein said gate element comprises a stacked gate structure comprising a floating gate 204, a control gate 206, and an oxide-nitride-oxide layer 208 between said floating gate 204 and said control gate 206. See col. 12, lines 59-65.

Conclusion

12. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
March 18, 2005